In the Claims:

Please cancel claims 17-22. Please add new claims 23-28. The claims are as follows.

1. (Original) An integrated circuit, comprising:

a predefined block of functional circuitry having a plurality of I/O pins; and

a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit.

2. (Original) The integrated circuit of claim 1, wherein said I/O pins are formed in a lower interconnect level of an integrated circuit chip.

3. (Original) The integrated circuit of claim 1, wherein said I/O pins are formed in a lowest interconnect level of an integrated circuit chip.

4. (Original) The integrated circuit of claim 1, wherein said integrated circuit is fabricated using a bulk silicon substrate or using a silicon-on-insulator substrate.

5. (Original) The integrated circuit of claim 1, wherein said predefined block of functional circuitry includes a first portion containing functional circuitry and a second portion containing said I/O pins.

6. (Original) The integrated circuit of claim 5, wherein said backside vias connect to said I/O pins in said second portion.

7. (Original) The integrated circuit of claim 1, further including:

a plurality of frontside I/O pads; and

additional I/O pins, each additional I/O pin electrically connected to one frontside I/O pad of the integrated circuit by a global wiring connection.

8. (Original) The integrated circuit of claim 1, further including non-predefined circuitry.

9. (Original) The integrated circuit of claim 8, further including:

a plurality of frontside I/O pads; and

said non-predefined circuitry having a plurality of I/O pins, each I/O pin of said non-predefined circuitry electrically connected to one frontside I/O pad of the integrated circuit by a global wiring connection.

10. (Original) The integrated circuit of claim 9, further including:

additional predefined circuit I/O pins, each additional predefined circuit I/O pin electrically connected to one frontside I/O pad of the integrated circuit by a global wiring connection.

11. (Original) A method of making electrical connection to an integrated circuit, comprising:

providing a predefined block of functional circuitry having a plurality of I/O pins; and

connecting a backside I/O pad electrically to each I/O pin through a backside via of the integrated circuit.

12. (Original) The method of claim 11, further including:

providing additional I/O pins; and

electrically connecting each additional I/O pin to one frontside I/O pad of the integrated circuit by a global wiring connection.

13. (Original) The method of claim 11, further including providing non-predefined circuitry.

14. (Original) The method of claim 13, further including:

providing a plurality of frontside I/O pads; and

electrically connecting one frontside I/O pad to a non-predefined circuit I/O pin by a global wiring connection.

15. (Original) The method of claim 14, further including:

providing additional predefined circuit I/O pins; and

electrically connecting each additional I/O pin to one frontside I/O pad of the integrated circuit by a global wiring connection.

16. (Original) The method of claim 11 further including:

forming said backside via in a bulk silicon substrate or a silicon on insulator substrate.

17-22. (Canceled)

23. (New) The integrated circuit of claim 1, further comprising:

a semiconductor substrate comprising semiconductor portions of devices;

a device level on the semiconductor substrate and in direct mechanical contact with the semiconductor substrate, wherein the device level includes non-semiconductor portions of said devices;

a first interconnect level on the device level and in direct mechanical contact with the device level; and

a second interconnect level on the first interconnect level and in direct mechanical contact with the first interconnect level, wherein the predefined block is a core comprising comprises a circuit portion and a redistribution portion, wherein the circuit portion includes all functional circuitry of the core, wherein the circuit portion includes a first portion of the substrate, a first portion of the device layer, a first portion of the first interconnect level, and a first portion of the second interconnect level, wherein the redistribution portion includes a second portion of the substrate, a second portion of the device layer, and a second portion of the first interconnect level, wherein the second portion of the substrate and the second portion of the device layer do not include any device, and wherein the plurality of I/O pins are contained in their entirety within the second portion of the first interconnect level in the redistribution portion.

24. (New) The integrated circuit of claim 23, wherein the backside via comprises:

a bulk conductor;

a conductor liner circumscribing the bulk conductor and in direct mechanical contact with the bulk conductor, wherein an I/O pin of the plurality of I/O pins is in direct mechanical and electrical contact with the conductor liner; and

an insulating liner circumscribing the conductor liner and in direct mechanical contact with the conductor liner, wherein the insulating liner insulates the bulk conductor from the semiconductor substrate.

25. (New) The integrated circuit of claim 1, wherein the backside via comprises:

a bulk conductor;

a conductor liner circumscribing the bulk conductor and in direct mechanical contact with the bulk conductor, wherein an I/O pin of the plurality of I/O pins is in direct mechanical and electrical contact with the conductor liner; and

an insulating liner circumscribing the conductor liner and in direct mechanical contact with the conductor liner, wherein the insulating liner insulates the bulk conductor from the semiconductor substrate.

26. (New) The method of claim 11, further comprising:

providing a semiconductor substrate comprising semiconductor portions of devices;

providing a device level on the semiconductor substrate and in direct mechanical contact with the semiconductor substrate, wherein the device level includes non-semiconductor portions of said devices;

providing a first interconnect level on the device level and in direct mechanical contact with the device level; and

providing a second interconnect level on the first interconnect level and in direct mechanical contact with the first interconnect level, wherein the predefined block is a core comprising comprises a circuit portion and a redistribution portion, wherein the circuit portion includes all functional circuitry of the core, wherein the circuit portion includes a first portion of the substrate, a first portion of the device layer, a first portion of the first interconnect level, and a first portion of the second interconnect level, wherein the redistribution portion includes a second portion of the substrate, a second portion of the device layer, and a second portion of the first interconnect level, wherein the second portion of the substrate and the second portion of the device layer do not include any device, and wherein the plurality of I/O pins are contained in their entirety within the second portion of the first interconnect level in the redistribution portion.

27. (New) The integrated circuit of claim 26, wherein the backside via comprises:

a bulk conductor;

a conductor liner circumscribing the bulk conductor and in direct mechanical contact with the bulk conductor, wherein an I/O pin of the plurality of I/O pins is in direct mechanical and electrical contact with the conductor liner; and

an insulating liner circumscribing the conductor liner and in direct mechanical contact with the conductor liner, wherein the insulating liner insulates the bulk conductor from the semiconductor substrate.

28. (New) The integrated circuit of claim 11, wherein the backside via comprises:

a bulk conductor;

a conductor liner circumscribing the bulk conductor and in direct mechanical contact with the bulk conductor, wherein an I/O pin of the plurality of I/O pins is in direct mechanical and electrical contact with the conductor liner; and

an insulating liner circumscribing the conductor liner and in direct mechanical contact with the conductor liner, wherein the insulating liner insulates the bulk conductor from the semiconductor substrate.